

Application No. 09/822,190
Reply to Office Action mailed March 15, 2004

Patent
Attorney Docket No. 85773-349

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (cancelled)
2. (cancelled)
3. (cancelled)
4. (currently amended) An apparatus suitable for ~~generating~~transmitting a signal for ~~transmission over a link between two ICs~~, said apparatus comprising:
 - a) an input for receiving an input signal comprising payload data to be transmitted ~~over the link between the two ICs~~;
 - b) a first processing unit coupled to said input, said first processing unit being operative for:
 - i) processing the payload data in the input signal to derive forward error correction data at least in part on the basis of the payload data in the input signal;
 - ii) generating ~~an output~~ a coded signal comprising the payload data received in the input signal and the forward error correction data generated in i);
 - c) ~~an output for releasing the output signal for transmission over a link between two ICs~~ a transmission link for transmitting the coded signal between the two ICs;
 - d) a second processing unit interfacing with said transmission link, said second processing unit being operative for processing the coded signal by extracting the payload data from the coded signal;

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- e) an output for releasing the payload data extracted by said second processing unit.
5. (currently amended) An apparatus as defined in claim 4, wherein ~~the said~~ transmission link between two ICs includes a backplane portion.
6. (currently amended) An apparatus as defined in claim 4, wherein said first processing unit is operative to apply BCH-1 coding on the payload data to derive the forward error correction data.
7. (currently amended) An apparatus as defined in claim 4, said first processing unit being further operative for:
- a) processing the input signal to generate N primary data structures, each primary data structure comprising a first portion and a second portion, the first portion including payload data and the second portion including forward error correction data derived from the payload data in the first portion of the primary data structure;
 - b) bit-multiplexing the N primary data structures generated in a) to derive a compound data structure;
 - c) generating a frame at least in part by grouping a plurality of compound data structures generated in b);
 - d) generating the ~~output~~ coded signal at least in part on the basis of the frame generated in c).
8. (currently amended) An apparatus suitable for ~~generating an output~~ transmitting a signal over a link between two ICs, said apparatus comprising:
- a) an input for receiving an input signal comprising data to be transmitted ~~over the link between the~~ two ICs;
 - b) a first processing unit coupled to said input for processing the input signal to generate ~~an output~~ a coded signal in which the data is organized into a sequence of frames, each frame including a plurality of sequential blocks,

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each block being characterized by a compound data structure suitable for carrying payload data and overhead information, said compound data structure being derived by bit-multiplexing a set of N primary data structures, each primary data structure comprising a first portion and a second portion, the first portion including payload data, the second portion including forward error correction data derived from the data elements in the first portion;

- c) ~~an output for releasing the output signal for transmission over a link between two ICs~~ a transmission link for transmitting the coded signal between the two ICs;
- d) a second processing unit interfacing with said transmission link, said second processing unit being operative for processing the coded signal by extracting the payload data from the coded signal;
- e) an output for releasing the payload data extracted by said second processing unit.

9. (currently amended) A method for ~~generating~~transmitting a signal for ~~transmission over a link between two ICs~~, said method comprising:

- a) receiving an input signal comprising payload data to be transmitted ~~over the link between the two ICs;~~
- b) processing the payload data in the input signal to derive forward error correction data at least on part on the basis of the payload data in the input signal;
- c) generating ~~an output~~ a coded signal comprising the payload data received in the input signal and the forward error correction data;
- d) ~~releasing output signal for transmission over the link between two ICs~~ transmitting the coded signal between the two ICs on a transmission link;
- e) interfacing with the transmission link in order to process the coded signal by extracting the payload data from the coded signal;
- f) releasing the payload data extracted from the coded signal.

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- 10.(currently amended) A method as defined in claim 9, wherein ~~the said~~ transmission link between two ICs includes a backplane portion.
- 11.(original) A method as defined in claim 9, wherein forward error correction data is derived at least in part by applying BCH-1 coding on the payload data.
- 12.(currently amended) A method as defined in claim 9, said method further comprising:
- a) processing the input signal to generate N primary data structures, each primary data structure comprising a first portion and a second portion, the first portion including payload data, the second portion including forward error correction data derived from the payload data in the first portion of the primary data structure;
 - b) bit-multiplexing the N primary data structures to derive a compound data structure, the compound data structure being suitable for carrying payload data and overhead information;
 - c) generating a frame at least in part by grouping a plurality of compound data structures;
 - d) generating the ~~output~~ coded signal at least in part on the basis of the frame generated in c).
- 13.(currently amended) A method for ~~generating an output~~ transmitting a signal for ~~transmission over a link between two ICs~~, said method comprising:
- a) receiving an input signal comprising data to be transmitted ~~over the link~~ between the two ICs;
 - b) processing the input signal to generate an ~~output~~ coded signal in which the data is organized into a sequence of frames, each frame including a plurality of sequential blocks, each block being characterized by a compound data structure suitable for carrying payload data and overhead information, said compound data structure being derived by bit-multiplexing a set of N primary data structures, each primary data structure comprising a first portion and a

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- second portion, the first portion including payload data, the second portion including forward error correction data derived from the data elements in the first portion;
- c) ~~releasing the output signal for transmission over a link between two ICs~~transmitting the coded signal between the two ICs on a transmission link;
 - d) interfacing with the transmission link in order to process the coded signal by extracting the payload data from the coded signal;
 - e) releasing the payload data extracted from the coded signal.

14.(cancelled)

15.(currently amended) ~~A signal~~ An apparatus as defined in claim ~~[[14]]4~~, wherein ~~the said transmission link~~ is between two ICs on a same circuit pack.

16.(cancelled)

17.(currently amended) ~~A signal~~ An apparatus as defined in claim ~~[[14]]7~~, wherein N is about 4.

18.(currently amended) ~~A signal~~ An apparatus as defined in claim ~~[[14]]4~~, ~~said wherein the coded signal having~~has a rate of about 2.5 Gb/s.

19.(currently amended) ~~A signal~~ An apparatus as defined in claim ~~[[14]]7~~, wherein each frame includes 66 sequential blocks and a framing pattern.

20.(currently amended) ~~A signal~~ An apparatus as defined in claim 19, wherein each primary data structure includes about 1176 bits.

21.(currently amended) ~~A signal~~ An apparatus as defined in claim 20, wherein at least part of the first 1164 bits of each primary data structure includes payload data, and 12 bits include forward error correction data.

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22.(currently amended) ~~A signal~~ An apparatus as defined in claim [[14]]7, wherein the forward error correction data in a given primary data structure are derived by applying BCH-1 coding on at least part of the payload data of the given primary data structure.